IN THE SPECIFICATION:

Please replace the paragraph beginning on page 1, lines 2-4 with the following replacement paragraph.

This application claims benefit of priority of now expired U.S. provisional application Serial No. 60/548,290 titled "Automatic Delays for the Alignment of Data and Digital Markers", filed February 27, 2004, and whose inventors are Neil S. Feiereisel and Craig M. Conway.

Please replace the paragraph beginning on page 13, paragraph [0038] with the following replacement paragraph.

[0038] In the embodiment illustrated in FIG. 1A, waveform generator 10 is an arbitrary waveform generator, and the ~~first signal 11~~second signal 12 is an analog signal and the ~~second signal 12~~first signal 11 is a digital marker signal. In this embodiment, waveform generator 10 may send the analog signal (e.g., the second signal 12) to stimulate a UUT 17, and may trigger another device, such as a high-speed digitizer 19, with the digital marker signal (e.g., the first signal 11).

Please replace the paragraph beginning on page 13, paragraph [0039] with the following replacement paragraph.

[0039] FIG. 1B illustrates a block diagram of one embodiment of a system comprising waveform generator 10 and a waveform generator 30 for generating a plurality of signals. It is noted that, as described above, each of waveform generators 10 and 30 may be any type of waveform generator. In one embodiment, the system may be operable to align signals from multiple sources. For example, in one embodiment, the system may be operable to align the output of a ~~first~~second signal 12 (e.g., an analog signal) provided by a first source (e.g. waveform generator 10) and the output of a ~~second~~third signal 32 (e.g., an analog signal) provided by a second source (e.g., waveform generator 30).

Please replace the paragraph beginning on page 13, paragraph [0039] with the following replacement paragraph.

[0040] In the embodiment illustrated in FIG. 1B, waveform generators 10 and 30 may be coupled together and may both be further coupled to a UUT 35. In one embodiment, some tests may require the UUT 35 to be stimulated by multiple signals simultaneously, even though the signals may have different signal characteristics. Therefore, in one embodiment, the system may comprise a delay determining unit which may be operable to determine a relative delay between the ~~first~~<u>second</u> signal 12 provided by waveform generator 10 and the ~~second~~<u>third</u> signal 32 provided by waveform generator 30, based upon a travel path of the ~~first~~<u>second</u> signal 12 and a travel path of the ~~second~~<u>third</u> signal 32. Furthermore, in one embodiment, the delay determining unit may be operable to program a delay circuit, based on a determined relative delay, to align the output of the ~~first~~<u>second</u> signal 12 with the output of the ~~second~~<u>third</u> signal 32 to test UUT 35.

Please replace the paragraph beginning on page 17, line 9 paragraph [0049] with the following replacement paragraph.

[0049] Marker path ~~103~~ <u>103a</u>, in one embodiment, may be the travel path for the digital marker signal 110. In one embodiment, marker path ~~103~~ <u>103a</u> may comprise a data pipeline delay compensation circuit ~~140~~ <u>140a</u> coupled to a delay determining unit 160 and a marker delay circuit ~~150~~ <u>150a</u>. Also, marker delay circuit ~~150~~ <u>150a</u> may be coupled to a status notification delay circuit ~~145~~ <u>145a</u>, delay determining unit 160, and digital logic ~~129~~ <u>129a</u>, which may coupled to a multiplexer 165. Additionally, in this embodiment, multiplexer 165 may be coupled to FPGA 141, which may further be coupled to output drivers 161-164. In one embodiment, digital marker 110 may be output from marker path ~~103~~ <u>103a</u> via any one of marker path I/O terminals 153-156. Furthermore, in one embodiment, circuit 101 may comprise a plurality of marker paths, for example, circuit 101 may comprise ~~marker path 103 and~~ marker paths ~~103b-103f~~ <u>103a-103f (103b – 103e being represented by the vertical dots in Figure 3)</u>, which are

similar to the illustrated marker path 103. In this example, as illustrated in FIG. 3, marker paths ~~103b-103f~~ 103a-103f may include data pipeline delay compensation circuits ~~140b-140f~~ 140a-140f (140b-140e being represented by the vertical dots in Figure 3), marker delay circuits ~~150b-150f~~ 150a-150f (150b-150e being represented by the vertical dots in Figure 3), digital logic circuits ~~129b-129f~~ 129a-129f (129b-129e being represented by the vertical dots in Figure 3), and status notification delay circuits ~~145b-145f~~ 145b-145e (145b-145e being represented by the vertical dots in Figure 3). In one embodiment, the plurality of marker paths are operable to output a plurality of digital markers via a plurality of marker path I/O terminals. For example, one or more of digital marker signals 110-115 may be output via marker path I/O terminals 153-156.

Please replace the paragraph beginning on page 28, line 22 paragraph [0076] with the following replacement paragraph.

[0076] Referring back to FIG. 3, in one embodiment, circuit 101 may be comprised in a single module. In another embodiment, circuit 101 may be formed by coupling a first module 101A to a second module 101B, shown demarcated in FIG. 3 by phantom line 180. In one embodiment, the first module 101A may be a base module, which may provide a common platform for delaying data signal and digital markers. In one embodiment, the second module 101B may be a daughter module, which may be, in one embodiment, an analog output module or, in another embodiment, a digital output module. In one embodiment, the delay determining unit 160 may determine the delay associated with the travel path of a particular type of daughter module to determine the relative delay, as described above. In one embodiment, the delay determining unit 160 may determine the delay associated with the travel path of a particular daughter module/base module combination to determine the relative delay, as described above. In one embodiment, as shown in FIG. 3, the base module may include at least one additional marker path I/O terminal 157 to output one or more digital markers (e.g., digital markers 110-115, with markers 111-114 being represented by the vertical dots) to be positioned with respect to data signal 105.

Please replace the paragraph beginning on page 32, paragraph [0085] with the following replacement paragraph.

[0085] Referring back to FIG. 1B, the ~~first~~second signal 12 provided by waveform generator 10 may be aligned in time with respect to the ~~second~~third signal 32 provided by waveform generator 30 to test a particular device (e.g., a UUT 35). In one embodiment, each of waveform generators 10 and 30 may be a standalone waveform generator or a computer-based waveform generator. In one embodiment, each of waveform generators 10 and 30 may be an arbitrary waveform generators or a digital waveform generator (i.e., logic signal source). Furthermore, in one embodiment, each of waveform generators 10 and 30 may comprise one embodiment of circuit 101 as illustrated in the embodiments of FIG. 3 and FIG. 6 and may comprise the functionality of circuit 101 as described in the above embodiments with reference to FIG. 3-7.

Please replace the paragraph beginning on page 32, paragraph [0086] with the following replacement paragraph.

[0086] In one embodiment, waveform generator 10 may be coupled to waveform generator 30. Waveform generators 10 and 30, in one embodiment, may be configured to receive user inputs specifying generation of signals. It is noted however that in other embodiments the signals may be created by other means, for example, by reproduction or modification of existing signals. In one embodiment, a delay determining unit, comprised in the system of FIG. 1B, may be operable to determine a relative delay between the ~~first~~second signal 12 (e.g., an analog signal) provided by the waveform generator 10 and the ~~second~~third signal 32 (e.g., an analog signal) provided by the waveform generator 30, based upon a travel path of the ~~first~~second signal 12 and a travel path of the ~~second~~third signal 32. Additionally, in one embodiment, the delay determining unit may be operable to program a data pipeline delay circuit, comprised in one of the waveform generators 10 and 30, based on the determined relative delay, to

delay the output of one of the first and second signals to align the output of the ~~first~~second signal 12 with the output of the ~~second~~third signal 32.

Please replace the paragraph beginning on page 33, paragraph [0087] with the following replacement paragraph.

[0087] FIG. 8 is a flow diagram illustrating a method for aligning the ~~first~~second signal 12 provided by waveform generator 10 and the ~~second~~third signal 32 provided by waveform generator 30. It should be noted that in various embodiments, some of the steps shown may be performed concurrently, in a different order than shown, or omitted. Additional steps may also be performed as desired.

Please replace the paragraph beginning on page 33, paragraph [0088] with the following replacement paragraph.

[0088] Referring collectively to FIG. 1B, FIG. 3, and FIG. 8, as indicated in 710, in one embodiment, a delay determining unit may automatically determine a total path delay associated with a travel path of the ~~first~~second signal 12 (e.g., an analog signal) and a total path delay associated with a travel path of the ~~second~~third signal 32 (e.g., an analog signal).

Please replace the paragraph beginning on page 33, paragraph [0089] with the following replacement paragraph.

[0089] In one embodiment, as indicated in 720, the delay determining unit may also automatically determine a relative delay between the ~~first~~second signal 12 and the ~~second~~third signal 32 by calculating the difference between the determined total path delay associated with the ~~first~~second signal 12 and the determined total path delay associated with the ~~second~~third signal 32.

Please replace the paragraph beginning on page 33, paragraph [0090] with the following replacement paragraph.

[0090] In 730, the delay determining unit may also automatically program a data pipeline delay circuit, such as data pipeline delay circuit 120 comprised in waveform generator 100 (as shown in FIG. 3), based on the determined relative delay, to delay the output of one of the signals 12 and 32 to align the output of the ~~first~~second signal 12 with the output of the ~~second~~third signal 32, according to one embodiment. As described below in more detail, in some embodiments, further delay criteria may be considered in the determination of the delay to be programmed, including, for example, user specified offsets.

Please replace the paragraph beginning on page 34, paragraph [0091] with the following replacement paragraph.

[0091] Lastly, in one embodiment, waveform generator 10 and waveform generator 30 may output the signals 12 and 32, respectively, as indicated in 740, where the output of the ~~first~~second signal 12 is preferably aligned in time or sample number with respect to the output of the ~~second~~third signal 32, in accordance with the determined relative delay. In one embodiment, the output of the ~~first~~second signal 12 is from a first data path I/O terminal comprised in waveform generator 10 and the output of the ~~second~~third signal 32 is from a second data path I/O terminal comprised in waveform generator 30. It is noted however that in other embodiments the delay determining unit may be operable to program a first data pipeline delay circuit comprised in waveform generator 10 and a second data pipeline delay circuit comprised in waveform generator 30 to align the output of the ~~first~~second signal 12 with the output of the ~~second~~third signal 32.

Please replace the paragraph beginning on page 34, paragraph [0092] with the following replacement paragraph.

[0092] In one embodiment, delay determining unit may be operable to receive a user input indicating an additional delay to program the data pipeline delay circuit to add the determined relative delay plus the additional delay to the output of the ~~first~~second signal 12 to output the ~~first~~second signal 12 at a predetermined position with respect to the output of the ~~second~~third signal 32. For example, the user input may indicate to add an additional delay of 6 samples to the output of the ~~first~~second signal 12. It is noted that in other embodiments a user may specify the additional delay in the waveform generators by entering a delay value in terms of time or number of samples.

Please replace the paragraph beginning on page 34, paragraph [0093] with the following replacement paragraph.

[0093] In one embodiment, delay determining unit may be operable to receive a user input reducing the determined relative delay to program the data pipeline delay circuit to add the reduced relative delay to the output of the ~~first~~second signal 12 to output the ~~first~~second signal 12 at a predetermined position with respect to the output of the ~~second~~third signal 32. For example, the user input may indicate to reduce the determined delay by 2 samples.

Please replace the paragraph beginning on page 35, paragraph [0094] with the following replacement paragraph.

[0094] In one embodiment, a user of waveform generator 10 may temporarily disable the automatic delay determining capabilities of delay determining unit. Instead, in this embodiment, the user may program the corresponding data pipeline delay circuit with a desired delay value to delay output of the ~~first~~second signal 12 to output the ~~first~~second signal 12 at a predetermined position with respect to the output of the ~~second~~third signal 32. In one embodiment, delay determining unit may be operable to receive a user input to program the corresponding data pipeline delay circuit with the desired delay value.

Please replace the paragraph beginning on page 36, line 20 paragraph [0099] with the following replacement paragraph.

[0098] In one embodiment, each of the waveform generators 10 and 30 may also include a plurality of data pipeline delay compensation circuits, similar to the embodiment of FIG. 3. For example, similarly to FIG. 3, in one embodiment, waveform generator 10 may include data pipeline delay compensation circuit 140 and data pipeline delay compensation circuits ~~140b-140f~~ 140a-140f. In one embodiment, each of the plurality of data pipeline delay compensation circuits in a particular waveform generator may be operable to delay one or more of a plurality of digital markers that may be output from the particular waveform generator. In one embodiment, the delay determining unit may be operable to program a data pipeline delay compensation circuit to delay the output of a digital marker signal which corresponds to a delayed data signal. In one embodiment, the delay data signal may be delayed by data pipeline delay circuit 120 to align the output of the delayed data signal with the output of another data signal; therefore, in response to the delay of the output of the delayed data signal, a data pipeline delay compensation circuit (e.g., data pipeline delay compensation circuit 140) may be programmed to compensate for the delay difference between the delayed data signal and the corresponding digital marker by delaying the output of the corresponding digital marker to align the output of the delayed data signal with the output of the corresponding digital marker.